Please replace the paragraph beginning on line 28 of page 9 with the following rewritten paragraph:

--FIG. 1 is a block diagram of one embodiment of a portion of a handset 50 for a mobile communication system. The handset 50 includes an input portion having a transducer 54 that receives an input signal 56, e.g., a voice or other acoustical signal, representing information to be communicated via the mobile communication system. The transducer 54 converts the input signal 56 into an electrical signal, typically an analog signal, which is supplied to an analog-to-digital converter (ADC) 58, for example a voice band ADC. The ADC 58 periodically samples the electrical signal and generates a sequence of multi-bit digital signals, which are supplied to a digital baseband processor 60. The baseband processor 60 performs further signal processing, including for example, compression. The output of the baseband processor 60 is supplied to burst store stage 62, which feeds a GMSK modulator 64. The GMSK modulator 64 produces multi-bit digital signals, which is supplied via signal lines, represented by a signal line 66, to a digital to analog conversion system 68. The digital to analog conversion system 68 converts the sequence of multi-bit digital signals into an analog signal, which is supplied via signal line 70 to an output portion 72. The output portion 72 includes a mixer 74 that receives the analog signal on signal line 70 and feeds a transmitter 76, which in turn transmits the signal. DAC can be used in any digital to analog conversion.--

Please replace the paragraph beginning on line 21 of page 20 with the rewritten paragraph shown below:

--FIG. 15 is a block diagram of another embodiment of the SC DAC (150), which is similar to the SC DAC 150 illustrated in FIGS. 9, 10A-10C, except that the SC DAC 150 of FIG. 15 further comprises a switch S48, a switch S49, and a switch S50. A first terminal of the switch S48 is connected to the second terminal of the charge sharing switch S43. A first terminal of the switch S49 is connected to the second terminal of the charge sharing switch S45. A first terminal of the switch S50 is connected to the second terminal of the charge sharing switch S46. Each of the switches S48, S49, and S50 may, but need not serve one or more of the functions noted hereinbelow. In one embodiment, one purpose of the switches S48, S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47.--

Please replace the paragraph beginning on line 31 of page 13 with the following rewritten paragraph:

--The DAC 150 may receive a non-overlapping 3-phase clock, P1, P2, P3, shown in FIG. 6. The closed/open condition of the switches S3, S6, S9, and S12 is controlled by the P3 signal of the 3-phase clock. The P1 signal of the 3-phase clock controls the open/closed condition of the charge sharing switches S13, S14, S15, and S16. The P2 signal of the 3-phase clock controls the open/closed condition of the switch S17.--

Please replace the paragraph beginning on line 13 of page 14 with the following rewritten paragraph:

--FIGS. 7A-7C are block diagrams showing the operation of the SC DAC 150 of FIG. 5 for each of the 3 clock phases in the event that input terminals 172, 178, 184, and 190 are supplied with digital bit signals bit_1, bit_2, bit_3, bit_4, having logic states of 1, 0, 0, 0, respectively. Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. In Fig. 7 and similarly labeled figures, the charges Q(C1)... Q(CN) represent the charge on capacitors C1... CN, respectively. Referring now to FIG. 7A, on phase P3 of the 3-phase clock, all of the charge sharing switches S13, S14, S15, and S16 and the output switch S17, are in the open condition. The capacitor C1 is charged to V_{ref} in response logic state 1 on terminal 172. Capacitors C2, C3 and C4 are all discharged to ground in response to the logic state 0 signals on terminals 178, 184, 190, respectively. Referring now to FIG. 7B, on phase P1 of the 3-phase clock, all of the charging switches S3, S6, S9 and S12 (FIG. 5) and the output switch S17 are in an open condition, and all of the charge sharing switches S13, S14, S15 and S16 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/4$. Referring now to FIG. 7C, on phase P2, charge sharing switches S14, S15, and S16 are in the open condition, output switch S17 is in the closed condition, and capacitor C1 (FIG. 5) of one-bit DAC 162 delivers its charge to the output

terminal 160. On the next occurrence of phase P3 (not shown), the multi-bit digital signal bit_1, bit_2, bit_3, and bit_4 may be updated and provided to the DAC 150 via input terminals 172, 178, 184, 190.--

Please replace the paragraph beginning on line 21 of page 25 with the following rewritten paragraph:

--FIG. 24 is a block diagram of one embodiment of a four bit scrambler 400 that receives a three bit digital input signal, bit_A, bit_B, bit_C, represented by the labeled arrows on the left, and outputs scrambled bits, represented by the arrows on the right. A scrambler is typically most effective when all of the scrambler inputs receive data . The extra input(s) of the scrambler may for example be "hardwired" to a logic state, i.e., a 1 or a 0. In this event that an input(s) of a scrambler is hardwired, it may be desirable to hardwire a corresponding number of DAC input(s), to a logic state opposite to that used for the extra input(s) of the scrambler.--

Please replace the paragraph beginning on line 6 of page 31 with the following rewritten paragraph:

FIG. 30 is a schematic diagram of one embodiment of the CT filter stage 92 of FIG. 2, which includes a two resistors R600, R601 that each receive an analog signal from the SC filter stage SCF, and form an RC filter with C600 and C601,to passively filter the images left by the switched capacitor filter. The images which appear at multiples of the SC filter sample rate. The stage may have selectable gain formed by an amplifier 600 and resistors R602-R607. The CT filter stage may further provide resistors R608, R609, which form a passive pole in combination with an off-chip capacitor C602. Although not required, the resistors in the output pole may be integrated to improve I/Q channel matching, reduce external component count and to reduce the effects of loading from the pin capacitance on the output stage amplifier.